What is Claimed Is:

1. A semiconductor device, comprising:

a plurality of memory cells each disposed at one of a plurality of intersections between a plurality of word lines and a plurality of data lines;

a plurality of first sense amplifiers each comprising a pair of MISFETs of a first conductivity type arranged to match each of said plurality of data lines;

a plurality of second sense amplifiers each comprising a pair of MISFETs of a second conductivity type and arranged to match each of said plurality of data lines;

a first power source supply line for supplying a first power source to said plurality of first sense amplifiers;

a first common source line where source nodes of said plurality of first sense amplifiers are commonly connected;

a second power source line for supplying a second power source to said plurality of second sense amplifiers;

a second common source line where source nodes of said plurality of second sense amplifiers are commonly connected;

a plurality of first switches provided between said first power source supply line and said first common source line;

a plurality of second switches provided between said second power source supply line and said second common source line;

a third power source supply line for supplying a third power source to said plurality of first sense amplifiers;

a third switch provided between said third power source supply line and said first common source line; and

a first output amplifier circuit connected with one of said data lines and having an input and an output separated from each other, whereby:

said first power source voltage is higher than said third power source voltage; and

said first output amplifier is activated earlier than said first and second sense amplifiers.

2. A semiconductor device according to claim 1, wherein:

when said first sense amplifier is activated, said first switch is changed to a conductive state, and then, said third switch is changed to a conductive state.

3. A semiconductor device according to claim 2, wherein:

a first region substantially rectangular in shape having an angle between first and second intersecting sides wherein said plurality of word lines, said plurality of data lines, and said plurality of memory cells are disposed in said first region;

a second region provided along said first side and comprising said plurality of first and second sense amplifiers, said plurality of first output amplifiers, said first and second power source supply lines, said first and second common source lines, and said plurality of first and second switches;

a third region arranged along said second side and comprising a plurality of connections between one of a plurality of word line driving circuits and one of said plurality of word lines; and

a fourth region comprising said third switch and sharing said angle in said first region where said first switch is disposed and wherein said fourth region is enclosed by said second and said third regions.

4. A semiconductor device, comprising:

a plurality of memory cells each disposed at one of a plurality of intersections of between a plurality of word lines and a plurality of first data lines;

a plurality of second data lines, said first and second data lines extending in a first direction;

a plurality of first sense amplifiers arranged between said pluralities of first and second data lines, each of said first sense amplifiers having a cross couple;

a plurality of second sense amplifiers connected between said plurality of first and second data lines, each of said second sense amplifiers having first and second inputs and first and second outputs wherein said first input is connected to said first data line between said first sense amplifier and one of a plurality of first MISFETs, said second input is connected to said second data line between said first sense amplifier and said one of said first MISFETs, said first and second outputs are connected to first and second data lines, respectively;

each of said plurality of first MISFETs having a source drain path connected between an input and an output of said plurality of second sense amplifiers; and

a first operating voltage supplied to said plurality of first sense amplifiers different from a second operating voltage supplied to said plurality of second sense amplifiers.

5. A semiconductor device according to claim 4, wherein each of said first sense amplifiers further comprises:

a second MISFET of first a conductivity type with a gate connected to one of said first data lines and with a drain connected to one of said second data lines;

a third MISFET of a first conductivity type with a gate connected to one of said second data lines and a drain connected to one of said first data lines; and

wherein each of said second sense amplifiers further comprises fourth and fifth MISFETs:

wherein said fourth MISFET of a first conductivity type has a gate connected to one of said first data lines between said first MISFET and said first sense amplifier and has a drain connected to one of said second data lines; and

a fifth MISFET of first conductivity type having a gate connected to said second data line between said first MISFET and said first sense amplifier and a drain connected to said first data line between said first MISFET and said memory cell.

6. A semiconductor device according to claim 5, wherein:

said first conductivity type is P-type, and said first operating voltage supplied to said plurality of first sense amplifiers is lower than operating voltage supplied to said plurality of second sense amplifiers.

7. A semiconductor device according to claim 5, wherein:

said first conductivity type is N-type, and said first operating voltage supplied to said plurality of first sense amplifiers is higher than said second operating voltage supplied to said plurality of second sense amplifiers.

8. A semiconductor device according to claim 4, wherein:

said device is controlled in such a manner that said second operating voltage supplied to said plurality of second sense amplifiers is equalized to said first operating voltage supplied to said plurality of first sense amplifiers after a first period of time.